

SIGNALS

Synthesis proves to be Holy Grail for analog EDA

Analog synthesis—the ability to construct efficient analog circuits from top-level descriptions—has become the holy grail of analog tool development. But the researchers pushing the envelope in synthesis are not to be found in whizzy corporate labs.

They are largely university people, toiling away on shoestring budgets and stubborn determination.

Significant progress appears to be coming from the work of four professors and their students: Rob Rutenbar and Richard Carley at Carnegie-Mellon University (Pittsburgh), Ranga Vemuri at the University of Cincinnati and Georges Gielen at the Catholic University of Leuven (Belgium).

Rutenbar's thinking on analog synthesis centers on the use of contemporary simulation tools. "It is difficult to get designers to trust the idea that synthesis actually works," he told *EE Times*. Manufacturers of analog and mixed-signal circuits have large investments in models and simulators, as well as qualification and sign-off flows. They are not looking to abandon Verilog of

update the search trees for usable circuits.

Carnegie-Mellon has gotten as many as 24 workstations to operate in parallel, said Rutenbar. The best topology for a power amplifier circuit, for example, with 100,000 alternatives came up in 10 CPU hours on a network of 20 Sun UltraSparcs. "That's the equivalent of five or six Spice runs for each circuit visited—or over a half-

lation accuracy for speed, in evaluating designs to synthesize. "For system-on-chip designs, that doesn't cut it," Rutenbar said. He noted that the Maelstrom and Anaconda tools will build accurate op amps, voltage references and other analog building blocks, though not complex signal modulators or phase-locked loops. But Rutenbar is confident that the ability to synthesize

these building blocks will give rise to the ability to build larger circuits.

Meanwhile, researchers at the Laboratory for Digital Design Environments at the University of Cincinnati have developed a "branch-and-bound" algorithm that automates an exhaustive search for alternative circuit topologies to synthesize. De-

Carnegie-Mellon's Rob Rutenbar plans to perform numerical circuit synthesis by attaching a "live" simulator to each circuit. Tools under development are designed to build very accurate op amps and other analog building blocks, opening the door to larger circuits.

signs are entered in VASE (VHDL-AMS Synthesis Environment); the synthesis process produces a net-list of sized components that optimizes circuit area and performance variables. Student researchers Adrian

